AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1 - 21. (canceled)

22. (currently amended) A signal processing integrated circuit comprising at least one channel and each channel comprising an input ~~coupled to an amplifier~~, wherein ~~the amplifier processes an input~~ at least one signal comes ~~coming~~ to ~~the~~ said input, each channel further comprising:

~~an~~ at least one amplifier coupled to said input for processing said ~~input~~ at least one signal and ~~outputting the~~ producing at least one amplified signal;

a processing circuit system for further processing ~~the~~ said at least one amplified signal and producing ~~outputting a~~ at least one processed signal;

a polarity switching circuit connected to at least one of said at least one amplifier;

~~a~~ at least one trigger circuit to produce at least one trigger signal using ~~the~~ said at least one processed signal ~~and output the said trigger signals~~; and

an output circuit system for outputting at least one of said at least one processed signal and said at least one trigger

signal ~~signals~~ responsive to said at least one ~~input~~ signal ~~signals, wherein a polarity switching circuit is connected to said amplifiers~~.

23. (previously presented) The integrated circuit of claim 22, wherein said polarity switching circuit is externally controlled.

24 - 27. (canceled)

28. (currently amended) A signal processing integrated circuit comprising at least one channel and each channel comprising an input ~~coupled to an amplifier~~, wherein ~~the amplifier processes an input~~ at least one signal comes ~~coming~~ to ~~the~~ said input, each channel further comprising:

~~an~~ at least one amplifier coupled to said input for processing said ~~input~~ at least one signal and ~~outputting the~~ producing at least one amplified signal;

a processing circuit system for further processing ~~the~~ said at least one amplified signal and producing ~~outputting a~~ at least one processed signal;

~~a~~ at least one trigger circuit to produce at least one trigger signal using ~~the~~ said at least one processed signal ~~and output the said trigger signals; and~~

at least one peak hold or sample and hold circuit coupled to said processing circuit system and producing at least one peak

hold or sample and hold signal; and

an output circuit system for outputting at least one of said at least one processed signal and said at least one trigger signal and at least one peak hold or sample and hold signal ~~signals~~ responsive to said at least one ~~input~~ signal ~~signals, further comprising a peak hold or sample and hold circuit coupled to output of at least one of said amplifiers~~.

29. (currently amended) A signal processing integrated circuit comprising at least one channel and each channel comprising an input ~~coupled to an amplifier~~, wherein ~~the amplifier processes an input~~ at least one signal comes ~~coming~~ to ~~the~~ said input, each channel further comprising:

~~an~~ at least one amplifier coupled to said input for processing said ~~input~~ at least one signal and ~~outputting the~~ producing at least one amplified signal;

a processing circuit system for further processing ~~the~~ said at least one amplified signal and producing ~~outputting a~~ at least one processed signal;

at least one comparator coupled to said processing circuit system and producing at least one comparator output signal;

~~a~~ at least one trigger circuit to produce at least one trigger signal using ~~the~~ at least one of said at least one comparator output signal and at least one processed signal ~~and output the said trigger signals~~; and

an output circuit system for outputting at least one of said at least one processed signal and said at least one trigger signal and at least one comparator output signal ~~signals~~ responsive to said at least one ~~input~~ signal ~~signals, further comprising a plurality of comparators connected to said amplifiers~~.

30. (previously presented) The integrated circuit of claim 29, wherein the said comparators can be at least one of following types; leading edge, zero crossing, constant fraction comparators.

31. (currently amended) The integrated circuit of claim 29, wherein ~~said plurality of~~ at least two comparators enclose at least one pulse height range of the said at least one signal ~~input signals~~.

32. (currently amended) The integrated circuit of claim 29 ~~30~~, ~~further comprising a circuit coupled to at least one of said plurality of comparators, said circuit producing~~ wherein at least one of said at least one comparator is a fast comparator to produce a fast trigger signal output.

33. (currently amended) The integrated circuit of claim 28, ~~further comprising a circuit connected to an output of~~ wherein output of said peak hold or sample and hold circuit is multiplexed through an analog bus to produce at least one output ~~to said~~

~~output circuit system~~.

34. (currently amended) The integrated circuit of claim 29, wherein an output of at least one output of said at least one comparator ~~plurality of comparators initiates~~ informs external circuitry to initiate a readout cycle of said signal processing integrated circuit.

35 - 38. (canceled)

39. (currently amended) A signal processing integrated circuit comprising at least one channel and each channel comprising an input ~~coupled to an amplifier~~, wherein ~~the amplifier processes an input~~ at least one signal comes ~~coming~~ to ~~the~~ said input, each channel further comprising:

~~an~~ at least one amplifier coupled to said input for processing said ~~input~~ at least one signal and ~~outputting the~~ producing at least one amplified signal;

a processing circuit system for further processing ~~the~~ said at least one amplified signal and producing ~~outputting a~~ at least one processed signal;

~~a~~ at least one trigger circuit to produce at least one trigger signal using ~~the~~ said at least one processed signal ~~and output the said trigger signals; and~~

a channel turn on and turn off system coupled to said

processing circuit system, wherein the said channel turn on and turn off system produces at least one of the two actions; turns on selected channels and turns off selected channels; and

an output circuit system for outputting at least one of said at least one processed signal from at least one turned on channel and said at least one trigger signal ~~signals~~ responsive to said at least one ~~input~~ signal ~~signals, wherein said output circuit system outputs a processed signal for one triggered channel of said plurality of integrated circuit channels and disables all remaining channels of said plurality of integrated circuit channels, wherein a time delay between said readout signal and said disablement of said remaining channels is controlled by an externally supplied signal~~.

40 - 43. (canceled)

44. (currently amended) The integrated circuit of claim 29, further comprising a first comparator of said at least one comparator ~~plurality of comparators~~ is a ~~low level~~ discriminator, and

wherein at least one of said first comparator produces an output trigger when pulse height of ~~the~~ said processed ~~input~~ at least one signal is larger than a first threshold voltage.

45. (currently amended) The integrated circuit of claim 29,

further comprising a second comparator of said at least one comparator ~~plurality of comparators~~ wherein said second comparator is an upper level discriminator, and

wherein said second comparator only produces a signal when pulse height of the said processed input signal is larger than a second threshold voltage.

46. (currently amended) A signal processing integrated circuit comprising at least one channel and each channel comprising an input ~~coupled to an amplifier~~, wherein ~~the amplifier processes an input~~ at least one signal comes ~~coming~~ to ~~the~~ said input, each channel further comprising:

~~an~~ at least one amplifier coupled to said input for processing said ~~input~~ at least one signal and ~~outputting the~~ producing at least one amplified signal;

a processing circuit system for further processing ~~the~~ said at least one amplified signal and producing ~~outputting a~~ at least one processed signal;

~~a~~ at least one trigger circuit to produce at least one trigger signal using ~~the~~ said at least one processed signal ~~and output the said trigger signals; and~~

a time difference measurement circuit connected to said processing circuit system for measuring the arrival time difference between different said at least one channel of said at least one signal coming to said input of each channel; and

an output circuit system for outputting at least one of said at least one processed signal and said at least one trigger signal and at least one time difference measurement ~~signals~~ responsive to said at least one ~~input~~ signal ~~signals, further comprising circuitry a time difference measurement circuit connected to the output circuit system for measuring the arrival time difference of said input signals between different channels~~.

47. (canceled)

48. (currently amended) The integrated circuit of claim 29, wherein ~~the plurality of~~ no comparators are used ~~is a single comparator~~.

49. (currently amended) The integrated circuit of claim 29, wherein at least one of said at least one comparator ~~the plurality of comparators~~ is a discriminator.

50. (currently amended) The integrated circuit of claim 29, wherein at least one of said at least one comparator ~~the plurality of comparators~~ is a fast comparator.

51 - 52. (canceled)

53. (currently amended) A signal processing integrated circuit comprising at least one channel and each channel comprising an input ~~coupled to an amplifier~~, wherein ~~the amplifier processes an input~~ at least one signal comes ~~coming~~ to ~~the~~ said input, each channel further comprising:

~~an~~ at least one amplifier coupled to said input for processing said ~~input~~ at least one signal and ~~outputting the~~ producing at least one amplified signal;

at least one pole zero cancellation circuit coupled to said at least one amplifier;

a processing circuit system for further processing ~~the~~ said at least one amplified signal processed by said at least one pole zero cancellation circuit and producing ~~outputting a~~ at least one processed signal;

~~a~~ at least one trigger circuit to produce at least one trigger signal using ~~the~~ said at least one processed signal ~~and output the said trigger signals~~; and

an output circuit system for outputting at least one of said at least one processed signal and said at least one trigger signal ~~signals~~ responsive to said at least one ~~input~~ signal ~~signals, further comprising a pole-zero cancellation circuit connected to the said amplifiers~~.

54 - 57. (canceled)

58. (currently amended) The integrated circuit of claim 46, ~~further comprising circuitry for measuring~~ wherein time difference measurement of said input signals between different channels was carried out by measuring the phase difference of a Sine and a Cosine wave simultaneously sent to each of said at least one channel ~~at the time when the said channel produces a trigger~~.

59. (currently amended) A signal processing integrated circuit comprising at least one channel and each channel comprising ~~an~~ at least one input, wherein at least one ~~input~~ signal comes to said at least one input, each channel further comprising:

~~an~~ at least one amplifier coupled to said at least one input processes said ~~input~~ at least one signal and ~~outputs the~~ produces at least one amplified signal;

a processing circuit system further processes said at least one amplified signal and ~~outputs~~ produces at least one processed signal;

~~a~~ at least one trigger circuit produces at least one trigger signal using said at least one processed signal; ~~and outputs said at least one trigger signal,~~

a control system configures and controls said integrated circuit ~~the functions,~~; and

an output system ~~for outputting~~ outputs at least one of said at least one processed signal and at least one trigger signal responsive to said at least one ~~input~~ signal.

60. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one shaping amplifier with externally selectable at least one shaping time.

61. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one polarity switching circuit.

62. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one pole zero circuit.

63. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one integration circuit.

64. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one differentiating circuit.

65. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one shaping circuit ~~amplifier~~.

66. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one gain amplifier.

67 - 68. (cancel)

69. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one peak hold circuit.

70. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one comparator circuit.

71. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one discriminator circuit.

72. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one digital to analog converter (DAC) circuit.

73. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one analog to digital converter (ADC) circuit.

74. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one baseline restoration circuit.

75. (currently amended) The integrated circuit of claim [[59]] 29, wherein said processing circuit includes at least one amplifier.

76. (currently amended) The integrated circuit of claim [[59]] 29, wherein said at least one amplifier coupled to said input is ~~a~~ at least one charge sensitive amplifier.

77. (currently amended) The integrated circuit of claim [[59]] 29, wherein said at least one amplifier is a transconductance amplifier ~~circuit~~.

78. (currently amended) The integrated circuit of claim 76 [[59]], wherein said charge sensitive amplifier includes at least one active resistance feedback circuit.

79. (currently amended) The integrated circuit of claim 76 [[59]], wherein said charge sensitive amplifier includes at least one passive resistance feedback circuit.

80. (currently amended) The integrated circuit of claim 76 [[59]], wherein said charge sensitive amplifier includes at least one transistor feedback circuit.

81. (currently amended) The integrated circuit of claim 76 [[59]], wherein said charge sensitive amplifier includes at least one MOSFET feedback circuit.

82. (currently amended) The integrated circuit of claim 76 [[59]], wherein said charge sensitive amplifier includes at least one capacitance feedback circuit.

83. (currently amended) The integrated circuit of claim 76 [[59]], wherein said charge sensitive amplifier includes at least one gain selection.

84. (currently amended) The integrated circuit of claim 76 [[59]], wherein said charge sensitive amplifier includes at least one offset adjustment circuit.

85. (currently amended) The integrated circuit of claim 76 [[59]], wherein said charge sensitive amplifier includes a self reset circuit.

86. (currently amended) The integrated circuit of claim 76

[[59]], wherein said charge sensitive amplifier includes at least one input capacitance optimization.

87. (currently amended) The integrated circuit of claim 59, wherein said amplifier includes at least one shaping circuit.

88. (currently amended) The integrated circuit of claim [[59]] 29, wherein said at least one trigger circuit includes at least one comparator.

89. (currently amended) The integrated circuit of claim [[59]] 29, wherein said at least one trigger circuit includes at least one discriminator.

90. (currently amended) The integrated circuit of claim [[59]] 29, wherein said at least one trigger circuit includes at least one differentiator.

91. (currently amended) The integrated circuit of claim [[59]] 29, wherein said at least one trigger circuit includes at least one integrator.

92. (currently amended) The integrated circuit of claim [[59]] 29, wherein said at least one trigger circuit produces at least one fast trigger signal for ~~accurate~~ timing applications.

93. (currently amended) The integrated circuit of claim [[59]] 29, wherein said output circuit system outputs said at least one processed signal if the ~~processed signal~~ said at least one trigger circuit produces a trigger signal.

94. (new) A signal processing integrated circuit comprising at least one channel and each channel comprising at least one input, wherein at least one signal comes to said at least one input, each channel further comprising:

at least one amplifier coupled to said at least one input processes said at least one signal and produces at least one amplified signal;

at least one pulse shaping circuit coupled to at least one of said at least one amplifier produce at least one shaped signal from said at least one pulse shaping circuit;

a processing circuit system further processes said at least one shaped signal and produces at least one processed signal;

at least one trigger circuit produces at least one trigger signal using said at least one processed signal;

a control system configures and controls said integrated circuit; and

an output system outputs at least one of said at least one processed signal and at least one trigger signal responsive to said at least one signal.

95. (new) The integrated circuit of claim 29, wherein at least one digital to analog converter (DAC) circuit is used to adjust the gain of said at least one amplifier.

96. (new) The integrated circuit of claim 29, wherein at least one digital to analog converter (DAC) circuit is used to adjust the offset of said at least one amplifier.

97. (new) The integrated circuit of claim 29, wherein at least one digital to analog converter (DAC) circuit is used to adjust the threshold of said at least one comparator.

98. (new) The integrated circuit of claim 29, wherein there is at least one test input.

99. (new) The integrated circuit of claim 29, wherein at least one hit/read shift register is used to inform external circuitry the channels that produced a trigger.

100. (new) The integrated circuit of claim 99, wherein said at least one hit/read shift register is used to carry out sparse readout of channels that contain data.

101. (new) The integrated circuit of claim 100, wherein said at

least one hit/read shift register is used to sparse read out of pixel detectors.

102. (new) The integrated circuit of claim 100, wherein said at least one hit/read shift register is used to nearest neighbor read out of pixel detectors.

103. (new) The integrated circuit of claim 100, wherein said at least one hit/read shift register is used to global read out of pixel detectors.

104. (new) The integrated circuit of claim 100, wherein at least one of said at least one hit/read shift register is used to for fast triggers.

105. (new) The integrated circuit of claim 29, wherein said input is single-ended.

106. (new) The integrated circuit of claim 29, wherein said input is differential.

107. (new) The integrated circuit of claim 29, wherein said input polarity for each channel is independently set to receive negative or positive said at least one signal.

108. (new) The integrated circuit of claim 29, wherein the readout shift register is externally set to read out only the required channels.

109. (new) The integrated circuit of claim 29, wherein the input transistor is optimized for at least one detector capacitance, which is externally selectable.

110. (new) The integrated circuit of claim 29, wherein the input transistor is optimized for at least one detector capacitance, which is externally selectable.

111. (new) The integrated circuit of claim 29, wherein the current supply to the input transistor is externally adjustable.

112. (new) The integrated circuit of claim 29, wherein said processing circuit includes at least one sample and hold circuit.

113. (new) The integrated circuit of claim 29, wherein said processing circuit includes at least one track and hold circuit.